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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/044,295      | 01/11/2002  | Shigetsugu Okamoto   | 70904/56,851        | 6848             |

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EXAMINER

DEWITTE, CONRAD J

| ART UNIT | PAPER NUMBER |
|----------|--------------|
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2673

DATE MAILED: 11/19/2003

6

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/044,295

Applicant(s)

OKAMOTO, SHIGETSUGU

Examiner

Conrad J. DeWitte

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 January 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, 11, 12 and 16-19 is/are rejected.
- 7) ☒ Claim(s) 7-10, 12-15 and 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 January 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other:

## DETAILED ACTION

### *Specification*

1. The disclosure is objected to because of the following informalities:
  - Page 2, line 2: Applicant used “right angle” not “right angles”
  - Page 6, line 16: Applicant used “ununiformed”. It would be clearer if he used “heterogeneous”.
  - Page 7, line 1: Applicant used “invenetion” not “invention”
  - Page 7, lines 15-20: Applicants use “According to the structure, in a case where the memory element stores either of binary such as light/light-off, either of the switching elements (for example, combination of a p type transistor and an n type transistor), which make up the complementary inverter, is conducted.” It would be clearer as “According to the structure, in a case where the memory element stores binary data such as light/light-off, one of the switching elements that make up the complementary inverter (for example, the combination of a p type transistor and an n type transistor) is conducted.”
  - Page 11, lines 19-21: Applicant states in his brief description of the drawings that Figure 6 is “an explanatory drawing showing a relation between a combination of the ON resistance value/the OFF resistance value of the TFT and the power consumption.” The Examiner believes that this characterization of Figure 6 is not accurate. Instead, Figure 6 appears to be “a chart showing the relationship of the ON resistance value, the OFF resistance value, and the OLED resistance, to the parameter

alpha ( $\alpha$ ).” The Examiner requests that the Applicant review this portion of the specification and consider the Examiner’s suggested amendment.

- Page 12, lines 2, 5, 8, 11, 14, 17, 20 and 23: Applicant used “modification” not “modified”
- Page 13, line 1: Applicant used “modification” not “modified”
- Page 13, line 6: Applicant used “another prior art” not “prior art”
- Page 13, lines 9-10: Applicant used “FIG. 20 is a graph showing a time change of a potential stored by a memory element, in the pixel.” It would be clearer as “FIG. 20 is a graph showing the change with time of potential stored by a memory element in the prior art pixel.”
- Page 22, line 11: Applicant used “resistor of the TFTn2.” not “resistor of the TFTn2, respectively.”
- Page 25, line 12: Applicant used “%” not “percent”
- Page 31, lines 10-14: Applicant should revise this sentence in keeping with the 37 C.F.R. § 1.84(h)(5) objections to the drawings, *infra*.
- Page 41, line 22: Applicant used “TFTp3n4” not “TFTn4”

Appropriate correction is required.

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

*Drawings*

3. Figures 18, 19, 20, and 21 should each be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
4. The drawings are objected to because in Figure 2, the second data line 2<sub>(2)</sub> is mislabeled 2<sub>(1)</sub>. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.
5. The drawings are objected to under 37 CFR 1.84(h)(5) because Figure 4 shows modified forms of construction in the same view. The Examiner suggests renumbering Figure 4 to Figure 4A and adding a Figure 4B. Figure 4A should show V<sub>ref</sub> and V<sub>g</sub> as in the current Figure 4 (except without the (V<sub>g</sub>) and (V<sub>ref</sub>)). Figure 4B should then switch the locations of V<sub>ref</sub> and V<sub>g</sub>. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance. In addition to this correction, the Examiner requests that Applicant make the corresponding changes throughout the specification where it refers to current Figure 4.
6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because Figure 2 includes the following reference sign not mentioned in the description: 39. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

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7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign mentioned in the description: On page 20, line 7 of the specification, Applicant mentions ground potential  $V_g$  in reference to Figure 1. However, Fig. 1 does not include ground potential  $V_g$  (even though the figure does include reference potential  $V_{ref}$  and data potential  $V_d$ ). The Examiner suggests including ground potential  $V_g$  to Figure 1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Claim Objections***

8. Claim 18 objected to because of the following informalities: Applicant used “a first electrode” not “a first power electrode” in line 3 of the claim. Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

9. The following is a quotation of the second paragraph of 35 U.S.C. § 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 18 recites the limitation “the first power electrode” in lines 5-6 of the claim. There is insufficient antecedent basis for this limitation in the claim. Please see supra, the objection to claim 18 for a suggested correction.

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-6, 17, and 18 are rejected under 35 U.S.C. § 102(b) as being anticipated by Bell et al. (U.S. Pat. No. 4,996,523 A).

13. Regarding claim 1, Bell et al. discloses a memory-integrated display element comprising an optical modulation element provided in a pixel (col. 2, lines 66-68; Fig. 1, element 40); a memory element, provided in the pixel, which stores binary data, which indicates a value inputted to the optical modulation element (col. 3, lines 6-7; Fig. 1, elements 20, 40), wherein said memory element is arranged by connecting at least two inverters to each other in a loop manner, and an output of an output inverter, one of the inverters, which functions as an output end of the memory element, is directly connected to one end of the optical modulation element (col. 4, lines 1-19; Fig. 3, elements 36, 38; Fig. 4, elements 33, 35).

14. Regarding claim 2, Bell et al. further discloses that said optical modulation element is a current drive type optical modulation element whose luminous intensity varies in accordance with a current quantity. Col. 3, lines 43-45; col. 4, lines 31-33; Fig. 1, elements 28, 40.

15. Regarding claim 3, Bell et al. further discloses that said optical modulation element is an Organic Light Emission Diode. Col. 4, lines 31-33.

16. Regarding claim 4, Bell et al. further discloses an electric charge emitting means for emitting electric charge, which has been stored in the optical modulation element while the

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memory element was applying a voltage to the optical modulation element, after the memory element finishes applying the voltage. Col. 2, line 66-68; Fig. 1, element 40 (note that the cathode end of the OLED is grounded, providing a charge emitting means).

17. Regarding claim 5, Bell et al. further discloses wherein said output inverter is a complementary inverter. Col. 4, lines 1-19.

18. Regarding claim 6, Bell et al. further discloses that said complementary inverter includes a p type transistor connected to a first power line (Fig. 3, element 36; Fig. 4, line 33); and an n type transistor connected to a second power line (Fig. 3, element 36; Fig. 4, line 33), and an anode of the optical modulation element is connected to an output end of the output inverter, and a cathode of the optical modulation element is connected to the second power line (col. 2, lines 66-68; Fig. 2, element 40).

19. Regarding claim 17, Bell et al. further discloses that said memory element includes a power electrode, which is used also as either of an anode or a cathode of the optical modulation element. Fig. 1, element 40; Fig. 3, element 36, 38.

20. Regarding claim 18, Bell et al. further discloses that said memory element includes a first power electrode and a second power electrode (Fig. 3, elements 36, 38; Fig. 4, elements 33, 35), and said optical modulation element includes an anode and a cathode (col. 4, lines 23-24 & 28-31); Fig. 5, element 40), and the first power electrode and the second power electrode are provided separately from the anode and the cathode. Col. 4, lines 1-11; Fig. 3, elements 36, 38.



***Claim Rejections - 35 USC § 103***

21. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

22. Claim 11 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Bell et al. as applied to claims 1 and 5 above, and further in view of Okumura et al. (U.S. Pat. No. 5,945,972 A).

Bell et al. discloses that said complementary inverter includes a p type transistor connected to a first power line (Fig. 3, element 36; Fig. 4, line 33); and an n type transistor connected to a second power line (Fig. 3, element 36; Fig. 4, line 33). Bell et al. fails to disclose a cathode of the optical modulation element is connected to an output end of the output inverter, and an anode of the optical modulation element is connected to the first power line.

However, Okayama et al. does disclose a cathode of the optical modulation element is connected to an output end of the output inverter, and an anode of the optical modulation element is connected to the first power line. Col. 2, lines 8-34; Fig. 1, elements 25, 10, 33, 34.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Bell et al. and Okumura et al. because both patents have the objective of controlling power consumption in a display through the use of control circuits. See Bell et al., at col. 1, lines 33-45; Okayama et al., at col. 23-29.

23. Claims 16 and 19 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Bell et al. as applied to claim 1 above, and further in view of Yamazaki et al. (U.S. Pat. No. 6,369,788 B1).

24. Regarding claim 16, Bell et al. fails to disclose that said optical modulation element and said memory element are included in each of plural sub pixels, which make up one pixel unit. However, Yamazaki et al. does disclose this feature. Col. 10, line 60-col. 11, line 10; Fig. 10A, elements 41-1, 41-2, 51-1, 51-2.

25. Regarding claim 19, Bell et al. discloses a plurality of data signal lines (col. 2, lines 51-62; Fig. 1, element 15; and a plurality of select signal lines which cross the data signal lines at right angles (col. 2, lines 51-62; Fig. 1, element 17), wherein said memory element is provided in each of combinations of the data signal lines and the select signal lines (col. 2, lines 51-68; Fig. 1, elements 12, 14, 16), and stores binary data indicated by a data signal line corresponding to the memory element, in a case where a select signal line corresponding to the memory element instructs the memory element to select (col. 2, lines 63-68; Fig. 1, elements 15, 17, 18, 20). Bell et al. does not disclose that the memory element is provided adjacent to another memory element, via a reference line, either of the data signal line and the select signal line, so that both memory elements are axially symmetrical with respect to the reference line, and the optical modulation element is provided adjacent to another optical modulation element, via the reference line, so that both optical modulation elements are axially symmetrical with respect to the reference line, and a power line is shared by the both memory elements, or the both optical modulation elements.

Yamazaki et al. does disclose that the memory element is provided adjacent to another memory element, via a reference line (Fig. 10A, element 52), either of the data signal line and the select signal line, so that both memory elements are axially symmetrical with respect to the reference line (col. 10, line 60-col. 11, line 10; Fig. 10A, elements 41-1, 41-2, 51-1, 51-2), and the optical modulation element is provided adjacent to another optical modulation element, via the reference line, so that both optical modulation elements are axially symmetrical with respect to the reference line (Fig. 10A, elements 52, 42), and a power line is shared by the both memory elements, or the both optical modulation elements (Fig. 10A, elements 48, 49).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Bell et al. and Yamazaki et al. because both patents have the objective of providing a display and a driving method for the display capable of displaying clear images. Bell et al., at col. 1, lines 48-57; Yamazaki et al., at col. 2, lines 17-19.

***Allowable Subject Matter***

26. Claims 7-10, and 12-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- Sekiya et al., U.S. Pat. No. 6,583,775 B1 (disclosing an image display apparatus)
- Schuler et al., U.S. Pat. No. 6,191,534 B1 (disclosing a low current drive of light emitting devices)
- Okayama, U.S. Pat. No. 6,127,718 A (disclosing a semiconductor device and method of manufacturing the same)
- Uemura et al., U.S. Pat. No. 4,688,030 A (disclosing a fluorescent display device)
- Prache, U.S. Pat. Appl'n No. 2002/0044110 A1 (disclosing a grayscale static pixel cell for OLED active matrix display)
- Koyama, U.S. Pat. Appl'n No. 2001/0002703 A1 (disclosing an electronic device)

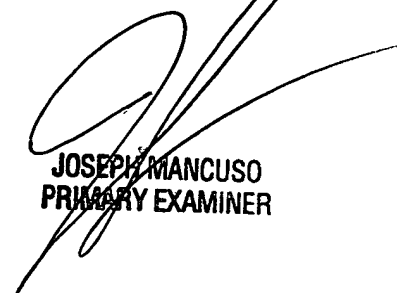
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Conrad J. DeWitte whose telephone number is (703) 305-8626. The examiner can normally be reached on Monday through Friday, 8 a.m. to 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.



CJD



JOSEPH MANCUSO  
PRIMARY EXAMINER